AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-19 (Canceled).

20. (Currently amended) A process for use in a manufacturing of application specific integrated circuits comprising the steps of:

providing a semi-fabricated semiconductor wafer that lacks a metal one layer and on which has been formed a plurality of circuits that comprise a logic design and at least one programmable circuit capable of performing at least one of a plurality of logic transfer functions upon programming;

determining modifications to the logic design that are desired by examining [[a]] an original specimen of the application specific integrated ~~circuits~~ circuit with a metal one layer;

determining desired changes in the metal one layer needed to implement the modifications in the logic design, including connecting the at least one programmable circuit to the plurality of circuits; and

forming a metal one layer on said semi-fabricated semiconductor wafer in the same location as the metal one layer of the original specimen but having a configuration different from the metal one layer of the original specimen to effect the desired changes.

21. (Previously Presented) The process of claim 20, wherein the act of forming the at least one programmable circuit comprises interconnecting the plurality of circuits by integrated circuit connection circuitry and connecting the at least one programmable circuit to the integrated circuit connection circuitry.

22. (Previously Presented) The process of claim 20, further comprising locating at least one configuration register on the semi-fabricated semiconductor wafer.

23. (Previously Presented) The process of claim 22 further comprising storing data for configuration signals in the at least one configuration register.

24. (Currently Amended) The process of claim 20, wherein the act of providing [[an]] a semi-fabricated semiconductor wafer with at least one programmable circuit comprises providing at least one general purpose logic block that comprises the at least one programmable circuit.

25. (Previously Presented) The process of claim 20, wherein the act of determining whether modifications to the logic design are desired comprises testing a semiconductor wafer upon which the plurality of circuits have been interconnected by integrated circuit connection circuitry.

26. (Previously Presented) The process of claim 20, further comprising providing on the semi-fabricated semiconductor a configuration register for storing configuration information for the at least one programmable circuit.

27. (Previously Presented) The process of claim 20, wherein the act of providing an semi-fabricated semiconductor wafer with at least one programmable circuit comprises providing a plurality of general purpose logic blocks in a dispersed pattern on the wafer.

Claim 28 (Canceled).